CLAIMS

1. An output buffer apparatus comprising:

first and second power supply terminals;

an output terminal;

a main-buffer circuit including a plurality of first transistors each connected between said first power supply terminal and said output terminal and a plurality of second transistors each connected between said second power supply terminal and said output terminal;

a pre-buffer circuit including a plurality of first pre-drivers each driving one of said first transistors in accordance with a data signal and a plurality of second pre-drivers each driving one of said second transistors in accordance with said data signal;

a plurality of first sequential circuits, each receiving a first impedance adjusting signal in synchronization with said data signal to turn ON one of said first pre-drivers; and

a plurality of second sequential circuits, each receiving a second impedance adjusting signal in synchronization with said data signal to turn ON one of said second pre-drivers.

2. The output buffer apparatus as set forth in claim 1, wherein each of said first sequential circuits comprises a first D-type flip-flop for fetching said first impedance adjusting signal in synchronization with a falling edge of said data signal,

each of said second sequential circuits comprising a second D-type flip-flop for fetching said second impedance adjusting signal in synchronization with a rising edge of said data signal.

3. The output buffer apparatus as set forth in claim

1, wherein each of said first sequential circuits comprises a first latch circuit which is in a hold state when said data signal indicates a first value and is in a through state when said data signal indicates a second value,

each of said second latch circuits comprising a second latch circuit which is in a through state when said data signal indicates said first value and is in a hold state when said data signal indicates said second value.

4. The output buffer apparatus as set forth in claim 3, wherein each of said first latch circuits comprises:

a first transfer gate for receiving said first impedance adjusting signal, said first transfer gate being turned OFF and ON when said data signal indicates said first and second values, respectively;

first and second inverters connected in a first feedback loop connected to said first transfer gate; and

a second transfer gate inserted into said first feedback loop, said second transfer gate being turned ON and OFF when said data signal indicates said first and second values, respectively,

each of said second latch circuits comprising:

a third transfer gate for receiving said second impedance adjusting signal, said third transfer gate being turned ON and OFF when said data signal indicates said first and second values, respectively;

third and fourth inverters connected in a second feedback loop connected to said third transfer gate; and

a fourth transfer gate inserted into said second feedback loop, said fourth transfer gate being turned

OFF and ON when said data signal indicates said first and second values, respectively.

5. An output buffer apparatus comprising:

a power supply terminal;

a ground terminal;

an output terminal;

a main-buffer circuit including a plurality of P-channel MOS transistors each connected between said power supply terminal and said output terminal and a plurality of N-channel MOS transistors each connected between said ground terminal and said output terminal;

a pre-buffer circuit including a plurality of first pre-drivers each driving one of said P-channel MOS transistors in accordance with a data signal and a plurality of second pre-drivers each driving one of said N-channel MOS transistors in accordance with said data signal;

a plurality of first D-type flip-flops, each receiving a first impedance adjusting signal in synchronization with a falling edge of said data signal to turn ON one of said first pre-drivers; and

a plurality of second D-type flip-flops, each receiving a second impedance adjusting signal in synchronization with a rising edge of said data signal to turn ON one of said second pre-drivers.

6. An output buffer apparatus comprising:

a power supply terminal;

a ground terminal;

an output terminal;

a main-buffer circuit including a plurality of P-channel MOS transistors each connected between said power supply terminal and said output terminal and a plurality of N-channel MOS transistors each connected between said ground terminal and said output terminal;

a pre-buffer circuit including a plurality of first pre-drivers each driving one of said P-channel MOS transistors in accordance with a data signal and a plurality of second pre-drivers each driving one of said N-channel MOS transistors in accordance with said data signal;

a plurality of first latch circuits, each receiving a first impedance adjusting signal to turn ON one of said first pre-drivers, each of said first latch circuits being in a hold state when said data signal indicates a first value and being in a through state when said data signal indicates a second value;

a plurality of second latch circuits , each receiving a second impedance adjusting signal to turn ON one of said second pre-drivers, each of said second latch circuits being in a through state when said data signal indicates said first value and being in a hold state when said data signal indicates said second value.

7. The output buffer apparatus as set forth in claim 6, wherein each of said first latch circuits comprises:

a first transfer gate for receiving said first impedance adjusting signal, said first transfer gate being turned OFF and ON when said data signal indicates said first and second values, respectively;

first and second inverters connected in a first feedback loop connected to said first transfer gate; and

a second transfer gate inserted into said first feedback loop, said second transfer gate being turned ON and OFF when said data signal indicates said first and second values, respectively,

each of said second latch circuits comprising:

a third transfer gate for receiving said second impedance adjusting signal, said third transfer gate

being turned ON and OFF when said data signal indicates said first and second values, respectively;

third and fourth inverters connected in a second feedback loop connected to said third transfer gate; and

a fourth transfer gate inserted into said second feedback loop, said fourth transfer gate being turned OFF and ON when said data signal indicates said first and second values, respectively.